Designing an Efficient Rail-to-Rail Class AB Amplifier as Buffer In LCD

SANA QURESHI, SAIMA AYYUB KHAN and PARESH RAWAT

Department of Electronics and Communication, Truba Institute of Science and Technology, Bhopal 462001, India.

(Received: February 05, 2015; Accepted: April 18, 2015)

ABSTRACT

For enhancing the high color depth and to provide higher resolution for LCD signal driver. This paper proposes a complementary differential amplifier with offset voltage cancellation technique. In order to improve the offset cancellation ability the complementary differential pairs are separated into main and auxiliary transconductance amplifiers. This achieves Rail-to-Rail output swing. In the proposed method offset cancellation is achieved by dividing offset cancellation and driving phases with the help of three switches. With this proposed architecture the offset voltage is reduced from 8.9 mV to 0.3 mV, which is a considerable amount of reduction. It is also observed that CMRR and Slew rate are not affected with the proposed technique

Key words: LCD, Amplifier, Signal driver, Rail-to-Rail.

INTRODUCTION

With increasing demand of LCD panel for high color depth and resolution it is hard to design a buffer with high resolution. The buffer has to match the speed, resolution, voltage swing and power dissipation of an LCD driver's to get high resolution. The resolution of the amplifier is dependent on the settling time the offset voltage and the slew rate.

The offset voltage is caused by the mismatch of the devices used in the circuit which limits the high-resolution of LCD driver. The general technique used to reduce the offset voltage is the output offset storage technique. However these two techniques introduce capacitors in the signal flow path. This is a serious issue in operational amplifiers and feedback systems. Parasitic capacitors thus formed can cause degradation of phase margin of the circuit thereby reducing stability of the circuit. So we have to design a circuit in such a manner that the offset cancellation technique should not come in the way of signal flow path.

We generally design a buffer with push-pull output stage which consists of two complementary common source transistors allowing RAIL TO RAIL output voltage swing. The gates of two output transistors can be driven by two in phase AC signals
separated by DC voltage. In this paper single ended amplifiers are used to drive the two output devices to achieve offset cancellation and to drive push-pull output. We use class AB operation because no extra current paths are needed in this operation.

The equivalent circuit of the proposed two-stage amplifier is shown in Fig.1, where \( g_{m1} \) and \( g_{m2} \), \( R_{01} \) and \( R_{02} \), and \( C_{01} \) and \( C_{02} \) are the transconductances, output resistances, and output parasitic capacitances of the first-stage and second-stage amplifiers, respectively. \( C_{CS} \) and \( R_{CS} \) are used for the stability of the circuit. The data line of the LCD panel is an R-C distribution. To simplify the small-signal analysis, the data line is modeled as a first-order R-C circuit. Since the first stage amplifier contains dual complementary differential pairs, the value of \( g_{m1} \) depends on the input common-mode voltage.

**Design issues**

To evaluate this value of \( g_{m1} \), the input voltage is divided into low, middle, and high levels. When the input voltage is at the low level, the PMOS input transconductance amplifiers are operating and the NMOS input transconductance amplifiers are cut off, vice versa for the high-level inputs. All transconductance amplifiers can amplify the input signal when the input voltage is at the middle level. Hence, the value of \( g_{m1} \) can be expressed as

\[
\begin{align*}
\text{As the input voltage is at high-level:} & \quad g_{m1} = g_{map} + g_{man} + g_{mp} + g_{mn} \quad \ldots(1B) \\
\text{As the input voltage is at the middle level:} & \quad g_{m1} = g_{map} + g_{mp} \quad \ldots(1C)
\end{align*}
\]

As the input voltage is at low-level in equation (1) where \( g_{man}, g_{mp}, g_{map}, g_{mn} \) are the transconductance amplifiers \( G_{man}, G_{map}, G_{mp}, G_{mn} \) respectively. Since the transconductance of the first stage amplifier varies with the input common-mode voltage, the dc gain of the amplifier varies over the signal swing for large signals. The distortion will then be generated in a continuously large signal. To reduce the distortion encountered due to this variation, the input stage should be modified to a rail-to-rail constant \( gm \) differential amplifier. For an LCD driver application, the amplifier is used to buffer the step-wise signals. Hence, the constant \( gm \) design is not suitable.

The open-loop transfer function \( A_{ol}(s) \) can be obtained from Fig. 2 and the assumptions:

\[
\begin{align*}
A_{ol}(s) &= \frac{V_{ds} (s)}{V_{dd} (s)} \quad \ldots(2A) \\
&= A_{ol} \frac{1}{\omega_{p1}} \quad \ldots(2B)
\end{align*}
\]

Where

\[
\begin{align*}
A_{ol} &= g_{m1} g_{m2} R_{01} R_{02} \\
\omega_{p1} &= \frac{1}{C_{01} R_{01} R_{02}} \\
\omega_{p2} &= \frac{1}{C_{01} C_{02} R_{01} R_{02}} \\
\omega_{p3} &= \frac{1}{C_{01} C_{02}} (2 R_{L} - R_{c})
\end{align*}
\]
The zeros at $w_{z1}$ and $w_{z2}$ are contributed by the distributed load and the Miller compensation, respectively. The dominant pole $w_{p1}$ is due to the Miller compensation and the distributed R-C load. The first term of the denominator in (4) is arisen at the interface between the first and second stages. The output resistance of the first stage, $R_{01}$, is interacting with the Miller capacitance, $C_{CS}g_{m2}R_{02}$, at the interface. The second term is due to the output resistance of the second stage and the load capacitance. Since the load capacitance of the LCD data line can be the order of hundred pico-farads, the second term, $C_L R_{02}$, cannot be neglected in the LCD driver application.

The second non-dominant pole $w_{p2}$ is arisen at the output of the second stage amplifier with the Miller effect. For a conventional two-stage operational amplifier, the first term of the numerator in (5) is much smaller than the second one, resulting to that

$$w_{p2} = \frac{gm2}{C_L} \quad \ldots(8)$$

That is: $w_{p2}$ is determined by the transconductance of the second stage amplifier and the load capacitance. Here, for the LCD driver application, the load capacitance cannot be neglected. If is much greater than $C_{CS}g_{m2}R_{01}$, $w_{p2}$ can be approximately expressed as: $1/C_{CS}R_{01}$, which is independent on the transconductance of the second stage amplifier and the load capacitance. The third and fourth nondominant poles $w_{p3}$ and $w_{p4}$ due to the parasitic capacitances, are far away from the other poles and zeros. Hence, they have less effect on the stability. The unity-gain frequency can be approximately expressed as

$$w_1 = A_{dz} w_{p1} = \frac{g_{m1}g_{m2}R_{01}R_{02}}{C_{CS}g_{m2}R_{CS} + C_L R_{02}} \quad \ldots(9)$$

which is larger than the second pole

Hence, the actual value of the unity-gain frequency is slightly smaller than that of (8). The position of $w_{z1}$ is greatly affected by the R-C load. The larger the load connected to the amplifier, the smaller the value of $w_{z1}$ decreasing to less than the unity-gain frequency for a large load.

Fig. 2: Schematic of proposed buffer with offset cancellation using LTSpice
**Proposed amplifier design**

The auxiliary transconductance amplifiers are used to extend the input swing. They can also be used for the offset cancellation. The architecture of the proposed amplifier without an offset cancellation is shown in Figure 2, and the architecture of the proposed amplifier with an offset cancellation is shown in Figure 4.4 where an offset storage capacitor and three switches are used in the circuit, and $V_{OS1}$, $V_{OS2}$, $V_{OS3}$, and $V_{OS4}$ are the input-referred offset voltages of $G_{map}$, $G_{mn}$, $G_{man}$, and $G_{mp}$, respectively.

Since the input stage contains both PMOS and NMOS differential amplifiers, the offset voltage varies with the input voltage. For the LCD driver application, a step-wise signal is applied to the input of the buffer amplifier. Hence, the buffer amplifier must sample each voltage level for the offset cancellation. The operation is divided into offset cancellation and driving phases. Before each driving phase, the amplifier is in the offset cancellation phase, the switches SW2 and SW3 are turned on, and the switch SW1 is turned off. After the offset cancellation is finished, SW1 is turned on and SW2 and SW3 are turned off. The circuit is then ready to drive its load.

During the offset cancellation phase, a negative feedback loop consisting of the auxiliary transconductance amplifiers, $G_{map}$ and $G_{man}$ the transimpedance amplifiers, $R_1$ and $R_2$, and the output transistors, M25 and M26, is formed. The input voltage is applied to the inverting input terminals of all transconductance amplifiers and to the non-inverting input terminals of the two main transconductance amplifiers. As depicted in Figure 3, the input-referred offset voltages $V_{OS1}$, and $V_{OS2}$, are applied to the two inputs of $G_{map}$ and $G_{man}$, respectively. The relation between the input and output voltages can be expressed as

$$V_{out} = \frac{\left( \pm V_{OS1} G_{map} + (V_{in} \pm V_{OS1}) G_{man} \right) R_1 + R_2}{\left( \pm V_{OS2} G_{map} + (V_{out} \pm V_{OS2}) G_{man} \right) R_2}$$

... (10)

where $g_{m25}$ and $g_{m26}$ are the transconductances of M25 and M26, respectively, and $R_2$ is the output resistance of the amplifier. Assume $g_{m25} = g_{m26}$ and $R_1 = R_2$ then

$$V_{out} = \frac{V_{in} \left( g_{map} g_{m25} R_1 + g_{man} g_{man} R_2 \right) \pm V_{OS1} g_{map} g_{man} R_1 \pm V_{OS2} g_{map} g_{man} R_2}{g_{map} g_{map} R_1 + g_{man} g_{man} R_2}$$

... (11)

Assume $g_{m25} = g_{m26}$ and $R_1 = R_2$ then

$$V_{out} = \frac{\pm V_{OS1} g_{man} \pm V_{OS2} g_{man}}{g_{map} + g_{man}}$$

... (12)
When SW2 and SW3 were off and SW1 is on, the output voltage is stored at the capacitance called as output offset voltage is

$$V_{out} - V_{in} \approx \pm V_{os1} g_{mn} \pm V_{os2} g_{mp} \frac{g_{map}}{g_{map} + g_{man}}$$ \hspace{1cm} (13)

The total output of the voltage referred to the input is given as

$$V_{OS.osc} = \frac{V_{out} - V_{in}}{A_{dc}} = \pm V_{os1} g_{mn} \pm V_{os2} g_{mp} \frac{g_{map}}{g_{map} + g_{man})A_{dc}}$$ \hspace{1cm} (14)

Where $A_{dc}$ is the DC gain of amplifier of the order of 80 dB. The switch SW2 will introduce injection induced either with generate, input referred offset voltage expressed as

$$V_{OS.inj} = \left( \frac{g_{map} + g_{man}}{g_{mn} + g_{mp}} \right) \Delta V$$ \hspace{1cm} (15)

Where "V" is the injection induced error on the storage capacitor to reduce the center the transconductance of the main transconductance amplifier is designed to be higher than auxiliary transconductance amplifier. In this methodology charge conservation technology is used to reduce the power consumption. In this methodology the data line are divided into three phases as in first phase all data lines are isolated from the output of the buffers. In second phase they are shorted with external capacitor $C_{ext}$. These first two phases are used for the charge conservation of the data lines. In the last phase, all data lines are connected to their corresponding buffer amplifiers, and the buffer amplifiers continue to drive the data lines to their final values. The charge conservation phase can also be used for the offset cancellation of the proposed amplifier, eliminating the need for an additional phase for offset cancellation. Thus, the driving time does not need to increase.

**Design process of buffer**

(A) Design Process (1/3)

Model Parameter Extraction
- $k_n, k_p$
- $\lambda_n, \lambda_p$
- $V_{thn}, V_{thp}$

all these can be get by process technology

Assign Current from Power Consumption Spec.
- Total Current : 3I mA
- Input pair : I mA
- Current mirror : 2I mA

(B) Design Process (2/3)

Determine W3 from CM_min, CM_max Spec.
- CM_min

| M1=3u/2u | M9=(4) | M17=3u/2u | M25=(4) |
| M2=(2) | M10=(2) | M18=3u/2u | M26=(2) |
| M3=(2) | M11=(2) | M19=3u/2u | Mr1=1u/7u |
| M4=(4) | M12=3u/2u | M20=3u/2u | Mr2=1u/7u |
| M5=(4) | M13=(2) | M21=3u/2u | Mr3=1u/7u |
| M6=3u/2u | M14=(2) | M22=3u/2u | Mr4=1u/7u |
| M7=3u/2u | M15=3u/2u | M23=3u/2u | Ccs1=.2pF, Ccs1=.2pF |
| M8=(4) | M16=3u/2u | M24=3u/2u | Cs=1pF |
$V_{dc} + V_{DSAT} + V_{GS1} = V_{dd} + V_{DSAT} + V_{DSAT} + V_{TH1}$

- **CM** \_**max**

Determine $W_{4-7}$ and Bias2 from $V_{out}$ \_**max** Spec.

- **V** \_**out** \_**max** : Determine $V_{B2}$

- Assign $V_{dsat}$ of $M4,5$ and $M6,7$ from $V_{out}$ \_**max** Spec

  *Eg* : $V_{out}$ \_**max** = 4V $\Rightarrow V_{dsat}$ of $M4,5$ = 0.6V, $V_{dsat}$ of $M6,7$ = 0.4V

- Calculate $W_{4-7}$ to satisfy $V_{dsat}$ and $I_{ds}$ of $M4-7$

- **V** \_**out** \_**min** = 0.8V $\Rightarrow V_{dsat}$ of $M8-11$ = 0.4V

- Calculate $W_{8-11}$ to satisfy $V_{dsat}$ and $I_{ds}$ of $M8-11$

**Design Process (3/3)**

- Determine $W_{1,2}$ from Gain Spec.

\[
R_0 = \frac{V_{X}}{I_{X}} = \left(\frac{g_m \cdot \tau_{47} \cdot (\tau_{02} || \tau_{03})}{g_m \cdot \tau_{09} \cdot \tau_{03}}\right)
\]

- Calculate Required $G_m$ value to satisfy Gain Spec.

- Gain = $G_m \cdot R_{out}$

- Calculate $W_{1,2}$ from $G_m$

- Check other Spec. and Repeat the design process to optimize transistors size

- Slew Rate

- **CM** \_**min** Check required

- CMRR, PSRR

**RESULTS**

Simulation and results are obtained using LTSPICE & MICROWIND software's. Results illustrate the tracking behavior of the proposed output buffer driven by a 50-kHz large-swing triangular wave and loaded with a large-size capacitance of 140pF. As can be inspected, the output voltage basically follows the input voltage for a full dynamic range. To show the output driving performance of the discussed buffer, results depicts the simulated transient response to a 50-kHz full-swing input step for the same capacitive load. Slew-rate values are found to be 12V/µs and 14V/µs for the rising and falling edges, respectively, whereas positive and negative settling time values within 100% of the final output voltage are only 3µs and 3.7µs, respectively. As can be observed, the output waveform follows the input waveform. The major performance parameters of the analyzed buffer are summarized and compared to other conventional topologies in Table 5, which shows a remarkable improvement of the proposed amplifier over other...

Fig. 5: Layout of the implemented buffer

Fig. 6: Input and output waveforms of the voltage
Table 2: Comparison Table for Offset Voltage Value

<table>
<thead>
<tr>
<th>Offset value without switches</th>
<th>Offset voltage with 3 switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.9 mV</td>
<td>0.3 µV</td>
</tr>
</tbody>
</table>

Table 4: Comparison Table for Slew Rate

<table>
<thead>
<tr>
<th>Slew rate without switches</th>
<th>Slew rate with 3 switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.5/2.4 V/µs</td>
<td>4.5/2.4 V/µs</td>
</tr>
</tbody>
</table>

Table 3: Comparison Table for CMRR (Common Mode Rejection Ratio)

<table>
<thead>
<tr>
<th>CMRR without switches</th>
<th>CMRR with 3 switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^{11.2}$</td>
<td>$10^{11.27}$</td>
</tr>
</tbody>
</table>

previously reported buffers. Figure 5 shows the layout of the analog buffer manually designed using Microwind. And the next diagram figure 6 shows its timing diagram. We can clearly see that output follows input. Table 2 compares the offset values using offset cancellation technique and without it. The method used for this work makes a huge difference in the offset voltage value. Similarly Tables 3 and 4 show that the inclusion of the three switches does not affect the CMRR and Slew Rate values.

CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB low offset buffer amplifier is implemented prosperously. Since the dissertation topic implements a very compact, high speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, additionally where slew rates is a matter of concern. Since it utilises a only 0.74 mV of static puissance, hence is having tremendous demand in hundreds of exhibit contrivances applications.

Due its merits, it can be utilized in following areas-

- Since power consumption is low, it has a great future in getting utilized in applications like "ultra low power ADCs".
- Since it is utilizing AMLCD technology, the exhibit is amended remarkably, hence can be utilized in "image exhibit contrivances, flat
panel exhibits etc.
• Due to rail-to-rail input and output cognations, it is greatly utilized in buffered analog clocks. Above are just few examples, but this buffer is having excellent usability in many other areas also.

• As with reduced offset it will be use full for high colour depth LCD panels means resolution of colour will increase significantly

REFERENCES


13. A New Compact Low-Power High-Speed Rail-to-Rail Class-B Buffer for LCD Applications Davide Marano, Gaetano Palumbo, Fellow, IEEE, and Salvatore Pennisi, Senior Member, ieee journal of display technology, 6(5), MAY 2010


